REMARKS

Claims 1-4, 6-8, 12-13, 15, and 20-22 remain for consideration. All claims are thought to be allowable over the cited art. Claims 1, 6, 8, 12, and 15 are amended for purposes of clarifying the invention and not for purposes of patentability. Claims 5, 9-11, 14, 16-19, and 23-43 are canceled without prejudice.

Response to Office Action

The current Office Action relies on "Kean" (US patent publication 2001/0037458 to Kean) in rejecting claims under 35 USC §102(e) and 35 USC §103(a). However, Kean is not thought to qualify as prior art because the filing date of Kean does not predate the filing date of the present application, and the Office Action does not show that the parent application of Kean (and the provisional upon which it is based) contains the same teachings as those cited in Kean.

However, assuming for purposes of argument only that the parent application of Kean contains the same teachings as those cited in Kean, the Office Action does not establish that claims 1-4, 12-16, 23-26, and 33-36 are anticipated under 35 USC §102(e) by "Kean". The rejection is respectfully traversed because the Office Action fails to show that Kean teaches all the limitations of the claims. However, the amendments made to independent claims 1 and 12 and the cancellation of claims 23-36 make the rejection moot.

Claim 1 is amended to include the limitations of claim 5 (now canceled), and claim 12 is amended to include the limitations of claim 19 (now canceled). As the Office Action acknowledges, Kean neither shows nor suggests the limitations of claims 5 and 19, and as explained below, the Office Action does not establish a *prima facie* case of obvious of these claims over the Kean-Pearson combination.

The Office Action fails to show that claims 5, 9, 17, 19, 27, 28, 37, and 41 are unpatentable under 35 USC §103(a) over Kean in view of "Pearson" (US patent number 5,838,256 to Pearson et al.). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Kean with teachings of Pearson, and fails to show that the combination could be made with a reasonable

likelihood of success. Claims 27-41 are canceled and the rejection is therefore moot for these claims.

As to claims 5 and 19 (now canceled and the limitations incorporated into claims 1 and 12, respectively), the Office Action fails to show that the Kean-Pearson combination suggests the limitations of and related to measuring propagation delays for a plurality of circuit elements on an FPGA and combining the propagation delays to generate a fingerprint. The cited teachings of Pearson at col. 7, l. 33 – col. 9, l. 25 neither teach nor suggest these limitations. This portion of Pearson apparently teaches a communication protocol (col. 7, l. 29). Further explanation of the communication protocol is provided in regards to write time slots, read time slots, 1-wire protocol, and device reset. There is no apparent reference in the discussion of the communication protocol to generating the fingerprint based on measuring propagation delays for a plurality of circuit elements on an FPGA and combining the propagation delays to generate a fingerprint. An explanation of those specific elements of Pearson thought to correspond to the claim limitations is requested if the rejection is maintained. Otherwise, the rejection should be withdrawn.

The Office Action newly cites the Web document entitled, "RFC 1750 - Randomness Recommendations for Security", ("RFC 1750") as evidence of random hardware techniques for generating a fingerprint. While this general statement may be true, there is no apparent suggestion by RFC 1750 of the specific claim limitations. That is, RFC 1750 does not appear to suggest the specific limitations of generating the fingerprint based on measuring propagation delays for a plurality of circuit elements on an FPGA and combining the propagation delays to generate a fingerprint.

The alleged motivation for modifying Kean with Pearson does not support *prima facie* obviousness. The alleged motivation simply states that it "would have been obvious because one skilled in the art would have been motivated by the suggestions provided by Pearson et al. so as to provide electronic key hardware module which is harder to crack, time-dependent operations, and more sophisticated random output function (columns 2-3)." This alleged motivation is insufficient because it is merely a broad, conclusory statement. There is no evidence presented to suggest which elements of the Kean could somehow be improved by specific elements of Pearson to

achieve the general objectives. Furthermore, even though the alleged statement may be a desirable general objective, there is no evidence of a motivation or suggestion to modify Kean in a manner consistent with the specific claim limitations. Therefore, the alleged motivation lacks clear and particular reasons that would lead one of ordinary skill in the art to combine specific teachings of Pearson with Kean.

As to claims 9 and 17, the Office Action fails to show that the Kean-Pearson combination suggests the limitations of and related to, in generating the fingerprint, determining whether a width of each line segment is less than a predetermined value; and generating, for each line segment, a corresponding bit of the fingerprint in response to the determining step. It is respectfully submitted that Pearson does not in any apparent way suggest determining a width of a line segment and generating a bit of the fingerprint in response to determination of the width. The cited teachings of Pearson at col. 8, l. 20-67 relate to Device Reset and have no apparent relevance to the claim limitations. Therefore, claims 9, 17, 28, and 41 are not shown to be unpatentable over the Kean-Pearson combination.

The rejection of claims 5, 9, 17, and 19 over the Kean-Pearson combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action fails to establish that claims 6-8, 20-22, 30-32, and 38-40 are unpatentable under 35 USC §103(a) over Kean in view of "Merritt" (US patent number 6,587,978 to Merritt et al.). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Kean with teachings of Merrit, and fails to show that the combination could be made with a reasonable likelihood of success. Claims 30-40 are canceled and the rejection is therefore moot for these claims.

Claims 6-8 include limitations of counting a number of oscillations of an oscillator in generating the fingerprint of the FPGA. The Office Action newly cites RFC 1750 as evidence that these limitations are well known in the art. This allegation is

respectfully traversed because the cited RFC 1750 apparently generally suggests "thermal noise or radioactive decay source and a fast, free-running oscillator" as a source for random numbers (section 5). The Office Action does not cite any specific teaching from RFC 1750 which shows how these generally named sources would be used in a manner suggestive of the specific claim limitations. Therefore, the specific claim limitations are not thought to be generally known.

The Office Action is mistaken in the allegation that Merrit teaches using an oscillator to generate a fingerprint. Merrit's col. 4, l. 22 – col. 5, l. 16 apparently teaches using an oscillator and associated circuitry to enable testing of a DRAM having lockout circuitry (also, col. 2, ll. 34-35). Merrit's test key circuitry is used to control various test functions (col. 5, ll. 20-22). Merrit's oscillator serves to enable testing of the DRAM, not generate a fingerprint. Furthermore, there is no suggestion of generating a fingerprint that represents an inherent manufacturing process characteristic unique to an FPGA.

Claims 8 and 22 include limitations of and related to the use of two oscillator counts in generating a fingerprint. The cited teachings of Merrit have no apparent relevance to these limitations. Reconsideration is respectfully requested. And if the rejection is maintained, an explanation of how specific elements of Merrit are understood to teach these limitations is requested.

Claims 20-22 are claims to an FPGA, and to the extent that the limitations of claims 20-22 are similar to those of claims 6-8, the Office Action does not show that the Kean-Merritt suggests the inventions claimed in claims 20-22.

The alleged motivation for modifying Kean with Merrit does not support *prima facie* obviousness. The alleged motivation simply states that it "would have been obvious because one skilled in the art would have been motivated by the suggestions provided by Merrit et al. so as to an electronic test key that varies pulse widths and/or periods, and frequencies of other control signals (column 7, lines 7-20) to stress, for instance, the memory device, it prevents failure on a simple test and it provide good production feedback as to where the lockout delays should be adjusted (column 6, lines 4-67) this implementation will eventually reduce costs and save valuable manufacturing time."

It is respectfully submitted that while these are statements made by Merritt for Merritt's invention, these reasons have no apparent relevance to the limitations of the present claims for generating a fingerprint. The alleged motivation is merely a broad conclusory statement of general applicability, and no evidence is provided to suggest the combination. Furthermore, the cited teachings of Merritt have no apparent relevance to the specific claim limitations. Therefore, the alleged motivation is insufficient to support *prima facie* obviousness.

The rejection of claims 6-8 and 20-22 over the Kean-Merrit combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action does not establish that claims 10-11, 18, 29, and 42-43 are unpatentable under 35 USC §103(a) over Kean in view of US patent number 6,185,126 to Rogers et al. (hereinafter, "Rogers"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Kean with teachings of Rogers, and fails to show that the combination could be made with a reasonable likelihood of success. Claims 29-43 are canceled and the rejection is therefore moot for these claims.

The Office Action fails to show that Rogers suggests the limitations of claims 10-11. Claims 10-11 include limitations of, among other limitations, using differences in transistor threshold voltages caused by manufacturing process variations to generate a fingerprint.

Rogers' teachings are for "setting the power-up state of some or all of the storage elements of a RAM-based FPGA or other programmable logic device to ensure that the proper state will be available immediately upon power up" (col. 1, l. 66 – col. 2, l. 3). Furthermore, the cited portion of Rogers teaches that the different threshold voltages of two transistors in a RAM cell are used to program a lookup table in the FPGA (col. 2, ll. 13-30). The claims make clear, and those skilled in the art will recognize that the claimed fingerprint is used to decrypt/encrypt the configuration data,

and individual bits of the fingerprint are not used to program the FPGA as the Office Action seems interpret the claim limitations.

Claim 18 is a claim to an FPGA having similar limitations to those of claims 10 and 11. Therefore the Office Action does not show that the Kean-Rogers combination suggests the limitations of claim 18 for at least the reasons set forth above for claims 10 and 11.

The alleged motivation for modifying Kean with Rogers does not support *prima facie* obviousness. The alleged motivation simply states that it "would have been obvious because one skilled in the art would have been motivated by the suggestions provided by Rogers et al. so as to encode the key signal by implementing embedded macrofunctions and allowing the logic so implemented to be available immediately upon power-up thus eliminate the need for a separate programming operation following power-up." This alleged motivation is insufficient because it is merely a broad, conclusory statement and lacks clear and particular reasons that would lead one of ordinary skill in the art to combine specific teachings of Rogers with Kean. Furthermore, the cited teachings of Rogers have no apparent relevance to the specific claim limitations.

Therefore, the alleged motivation is insufficient to support *prima facie* obviousness.

The rejection of claims 10-11, 18, 29, and 42-43 over the Kean-Rogers combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

Response to Advisory Action

In the Advisory Action the Examiner did not enter the amended claims because the Examiner stated that they raised new that will need further consideration and search. In addition the Examiner argued that Pearson teaches generating a fingerprint (col. 2, line 39 through col. 3, line 4), which comprises measuring propagation delays for a plurality of circuit elements on an FPGA and combining them

to generate the fingerprint as discussed in col. 17, line 15 through col. 18, line 61 with emphasis for instance in col. 18, lines 9-15.

In Response to the Examiner not entering the amended claims the Applicant's submit this RCE with the above Response to the Final Office Action.

The Applicant also disagrees with the Examiners further comment that Pearson teaches generating a fingerprint, which comprises measuring propagation delays for a plurality of circuit elements on an FPGA and combining them to generate the fingerprint. Col. 2, line 39 through col. 3, line 4 of Pearson discusses various types of electronic keys. Col. 17, line 15 through col. 18, line 61 (including col. 18, lines 9-15) of Person discusses a power-on reset circuit (Fig. 12, col. 16, lines 60-64). The Power-on reset circuit 41in Fig. 12 is part of Figs. 5A and 5B, which are in turn part of Fig. 4A and 4B (see Brief Description of the Drawings in cols. 3 and 4). Figs. 4A and B represent the electronic key circuit. Thus the Examiner's citations in Pearson deal with a power-on reset circuit in an electronic key circuit.

Amended Claim 1 includes, among other features, generating a fingerprint within the FPGA, the fingerprint representing an inherent manufacturing process characteristic unique to the FPGA, wherein generating the fingerprint includes measuring propagation delays for a plurality of circuit elements on the FPGA and combining the propagation delays to generate the fingerprint. Pearson neither discloses nor teaches this feature. Pearson does not disclose an FPGA or using delay in a power-on reset circuit as a fingerprint as described in Claim 1. Thus this rejection should be withdrawn.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 10, 2005.

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